Pin and function listing for the Freescale HC9S12XDP512 chip and Technological Arts Adapt 9S12XDP512 card.

Legend
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Not on 112 pin	Does it?	Does it?	H1 header	H2 header	Can't use	Rearrangable	Both H1/H2	Unique function	Warning	Top side header	Input (normal config)	Output (normal config)	GPIO	Ignition output driving
	YES	NO							N/A					Input capture for rpm/engine position decoding

Adapt Pin	Module	CPU internal	Inner group	Outer group	MCU pin	Digital out	Digital in	Analog in	Hardware PWM	Precision timed	Interrupt cabability	Freescale intended use	Our use	Notes
30.	ATD0+ ATD1	VRH	N/A	N/A	VRH	N/A	N/A	N/A	N/A	N/A	N/A	Hi Referance Voltage for ATD	+5.0V	Possibly connect the main board 5v ldo supply here
31.	ATD0+ ATD1	VRL	N/A	N/A	VRL	N/A	N/A	N/A	N/A	N/A	N/A	Low Referance Voltage for ATD	Ground	Signal ground
22.	ATD0	AN0	DDRAD0	AD0	PAD00	NO	YES	YES	NO	NO	NO	Analog input	IAT – Inlet Air Temperature (Kelvin)	All these
23.	ATD0	AN1	DDRAD0	AD0	PAD01	NO	YES	YES	NO	NO	NO	Analog input	CHT – Coolant / Head Temperature (Kelvin)	yellow ones
24.	ATD0	AN2	DDRAD0	AD0	PAD02	NO	YES	YES	NO	NO	NO	Analog input	TPS – Throttle Position Sensor (%)	are swap
25.	ATD0	AN3	DDRAD0	AD0	PAD03	NO	YES	YES	NO	NO	NO	Analog input	EGO – Exhaust Gas Oxygen (lambda)	able to suit
29.	ATD0	AN4	DDRAD0	AD0	PAD04	NO	YES	YES	NO	NO	NO	Analog input	BRV – Battery Voltage Reference (Volts)	board layout
28.	ATD0	AN5	DDRAD0	AD0	PAD05	NO	YES	YES	NO	NO	NO	Analog input	MAP – Manifold Absolute Pressure (kPa)	needs at
27.	ATD0	AN6	DDRAD0	AD0	PAD06	NO	YES	YES	NO	NO	NO	Analog input	AAP – Atmospheric Absolute Pressure (kPa)	the designers
26.	ATD0	AN7	DDRAD0	AD0	PAD07	NO	YES	YES	NO	NO	NO	Analog input	MAT – Manifold Air Temperature (Kelvin)	whim.
22.	ATD1	AN8	DDRAD1	AD1	PAD08	NO	YES	YES	NO	NO	NO	Analog input	EGO2 – Exhaust Gas Oxygen 2 (lambda)	All these
23.	ATD1	AN9	DDRAD1	AD1	PAD09	NO	YES	YES	NO	NO	NO	Analog input	IAP – Intercooler Absolute Pressure (kPa)	yellow ones
24.	ATD1	AN10	DDRAD1	AD1	PAD10	NO	YES	YES	NO	NO	NO	Analog input	MAF – Mass Air Flow (gm/sec/dimensionless)	are swap
25.	ATD1	AN11	DDRAD1	AD1	PAD11	NO	YES	YES	NO	NO	NO	Analog input	SpareADC3 (ADC1 3)	able to suit
29.	ATD1	AN12	DDRAD1	AD1	PAD12	NO	YES	YES	NO	NO	NO	Analog input	SpareADC4 (ADC1 4)	board layout
28.	ATD1	AN13	DDRAD1	AD1	PAD13	NO	YES	YES	NO	NO	NO	Analog input	SpareADC5 (ADC1 5)	needs at
27.	ATD1	AN14	DDRAD1	AD1	PAD14	NO	YES	YES	NO	NO	NO	Analog input	SpareADC6 (ADC1 6)	the designers
26.	ATD1	AN15	DDRAD1	AD1	PAD15	NO	YES	YES	NO	NO	NO	Analog input	SpareADC7 (ADC1 7)	whim.
13.	ECT	IOC0	DDRT	PTT	PT0	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Primary engine rpm/position sensor input	Input capture mode for best accuracy (0-3 are buffered and more)
12.	ECT	IOC1	DDRT	PTT	PT1	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Secondary engine rpm/position sensor input	Input capture mode for best accuracy (0-3 are buffered and more)
11.	ECT	IOC2	DDRT	PTT	PT2	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Injector out 1 in OC mode for best accuracy	More than 6 cylinders will be fired with two shots per engine cycle, both timed. Sequential

														to 6 cylinders, semi sequential to 12 cylinders
10.	ECT	ICO3	DDRT	PTT	PT3	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Injector out 2 in OC mode for best accuracy	More than 6 cylinders will be fired with two shots per engine cycle, both timed. Sequential to 6 cylinders, semi sequential to 12 cylinders
9.	ECT	ICO4	DDRT	PTT	PT4	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Injector out 3 in OC mode for best accuracy	More than 6 cylinders will be fired with two shots per engine cycle, both timed. Sequential to 6 cylinders, semi sequential to 12 cylinders
8.	ECT	IOC5	DDRT	PTT	PT5	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Injector out 4 in OC mode for best accuracy	More than 6 cylinders will be fired with two shots per engine cycle, both timed. Sequential to 6 cylinders, semi sequential to 12 cylinders
7.	ECT	IOC6	DDRT	PTT	PT6	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Injector out 5 in OC mode for best accuracy	More than 6 cylinders will be fired with two shots per engine cycle, both timed. Sequential to 6 cylinders, semi sequential to 12 cylinders
6.	ECT	IOC7	DDRT	PTT	PT7	YES	YES	NO	NO	YES	NO	Input capture/Output compare	Injector out 6 in OC mode for best accuracy	More than 6 cylinders will be fired with two shots per engine cycle, both timed. Sequential to 6 cylinders, semi sequential to 12 cylinders
48.	SCI0	RXD0	DDRS	PTS	PS0	YES	YES	NO	NO	NO	NO	SCI0 Rx	RS232 One – loading code and fast datalogging	This is required to be kept for loading code using the serial monitor as home brew setups will have to use this method.
5.	SCI0	TXD0	DDRS	PTS	PS1	YES	YES	NO	NO	NO	NO	SCI0 Tx	RS232 One – loading code and fast datalogging	This is required to be kept for loading code using the serial monitor as home brew setups will have to use this method.
34.	SCI1	RXD1	DDRS	PTS	PS2	YES	YES	NO	NO	NO	NO	SCI1 Rx	RS232 OR USB OR other comms for tuning etc	This could be used for main comms and the other for other stuff or vice versa, but my preference would be a more robust medium than RS232
32.	SCI1	TXD1	DDRS	PTS	PS3	YES	YES	NO	NO	NO	NO	SCI1 Tx	RS232 OR USB OR other comms for tuning etc	This could be used for main comms and the other for other stuff or vice versa, but my preference would be a more robust medium than RS232
1.	SPI0	MISO0	DDRS	PTS	PS4	YES	YES	NO	NO	NO	NO	SPI0 Master in	Reserved for onboard datalogging to flash	
2.	SPI0	MOSI0	DDRS	PTS	PS5	YES	YES	NO	NO	NO	NO	SPI0 Master out	Reserved for onboard datalogging to flash	
3.	SPI0	SCK0	DDRS	PTS	PS6	YES	YES	NO	NO	NO	NO	SPI0 Clock	Reserved for onboard datalogging to flash	
4.	SPI0	SS0	DDRS	PTS	PS7	YES	YES	NO	NO	NO	NO	SPI0 Slave select	Reserved for onboard datalogging to flash	
30.	CAN0	RXCAN0	DDRM	PTM	PM0	YES	YES	NO	NO	NO	NO	CAN0 Rx	Reserved for wired can tranceiver chip	
31.	CAN0	TXCAN0	DDRM	PTM	PM1	YES	YES	NO	NO	NO	NO	CAN0 Tx	Reserved for wired can tranceiver chip	
32.	CAN1	RXCAN1	DDRM	PTM	PM2	YES	YES	NO	NO	NO	NO	CAN1 Rx	Reserved for wired can tranceiver chip	
33.	CAN1	TXCAN1	DDRM	PTM	PM3	YES	YES	NO	NO	NO	NO	CAN1 Tx	Reserved for wired can tranceiver chip	

34.	CAN2	RXCAN2	DDRM	PTM	PM4	YES	YES	NO	NO	NO	NO	CAN2 Rx		
35.	CAN2	TXCAN2	DDRM	PTM	PM5	YES	YES	NO	NO	NO	NO	CAN2 Tx		
36.	CAN3	RXCAN3	DDRM	PTM	PM6	YES	YES	NO	NO	NO	NO	CAN3 Rx		
37.	CAN4	TXCAN3	DDRM	PTM	PM7	YES	YES	NO	NO	NO	NO	CAN3 Tx		
40.	SCI2	RXD2	DDRJ	PTJ	PJ0	YES	YES	NO	NO	NO	YES	SCI2 Rx	(with interrupt cabability)	
21.	SCI2	TXD2	DDRJ	PTJ	PJ1	YES	YES	NO	NO	NO	YES	SCI2 Tx	(with interrupt cabability)	
38.	IIC0	SDA0	DDRJ	PTJ	PJ6	YES	YES	NO	NO	NO	YES	IIC0 Data	Reserved for onboard clock time/date logging	
39.	IIC0	SCL0	DDRJ	PTJ	PJ7	YES	YES	NO	NO	NO	YES	IIC0 Clock	Reserved for onboard clock time/date logging	
21.	PWM	PWM0	DDRP	PTP	PP0	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	All these
20.	PWM	PWM1	DDRP	PTP	PP1	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	yellow ones
19.	PWM	PWM2	DDRP	PTP	PP2	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	are swap
18.	PWM	PWM3	DDRP	PTP	PP3	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	able to suit
17.	PWM	PWM4	DDRP	PTP	PP4	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	board layout
16.	PWM	PWM5	DDRP	PTP	PP5	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	needs at
15.	PWM	PWM6	DDRP	PTP	PP6	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	the designers
14.	PWM	PWM7	DDRP	PTP	PP7	YES	YES	NO	YES	NO	YES	Hardware PWM	Reserved for PWM applications (idle/boost/etc)	whim.
42.	SPI1	MISO1	DDRH	PTH	PH0	YES	YES	NO	NO	NO	YES	SPI1 Master in	Reserved for data transfer to other chips	
41.	SPI1	MOSI1	DDRH	PTH	PH1	YES	YES	NO	NO	NO	YES	SPI1 Master out	Reserved for data transfer to other chips	
40.	SPI1	SCK1	DDRH	PTH	PH2	YES	YES	NO	NO	NO	YES	SPI1 Clock	Reserved for data transfer to other chips	
39.	SPI1	SS1	DDRH	PTH	PH3	YES	YES	NO	NO	NO	YES	SPI1 Slave select	Reserved for data transfer to other chips	
38.	SPI2	MISO2	DDRH	PTH	PH4	YES	YES	NO	NO	NO	YES	SPI2 Master in	Reserved for data transfer to other chips	
37.	SPI2	MOSI2	DDRH	PTH	PH5	YES	YES	NO	NO	NO	YES	SPI2 Master out	Reserved for data transfer to other chips	
36.	SPI2	SCK2	DDRH	PTH	PH6	YES	YES	NO	NO	NO	YES	SPI2 Clock	Reserved for data transfer to other chips	
35.	SPI2	SS2	DDRH	PTH	PH7	YES	YES	NO	NO	NO	YES	SPI2 Slave select	Reserved for data transfer to other chips	
16.	EBI	ADDR0	DDRB	PTB	PB0	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 1	Bit banged using the down counting PIT timers
15.	EBI	ADDR1	DDRB	PTB	PB1	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 2	Bit banged using the down counting PIT timers
14.	EBI	ADDR2	DDRB	PTB	PB2	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 3	Bit banged using the down counting PIT timers
13.	EBI	ADDR3	DDRB	PTB	PB3	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 4	Bit banged using the down counting PIT timers

12.	EBI	ADDR4	DDRB	PTB	PB4	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 5	Bit banged using the down counting PIT timers
11.	EBI	ADDR5	DDRB	PTB	PB5	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 6	Bit banged using the down counting PIT timers
10.	EBI	ADDR6	DDRB	PTB	PB6	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 7	Bit banged using the down counting PIT timers
9.	EBI	ADDR7	DDRB	PTB	PB7	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 8	Bit banged using the down counting PIT timers
8.	EBI	ADDR8	DDRA	PTA	PA0	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 9	Bit banged using the down counting PIT timers
7.	EBI	ADDR9	DDRA	PTA	PA1	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 10	Bit banged using the down counting PIT timers
6.	EBI	ADDR10	DDRA	PTA	PA2	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 11	Bit banged using the down counting PIT timers
5.	EBI	ADDR11	DDRA	PTA	PA3	YES	YES	NO	NO	NO	NO	External address bus	Ignition out 12	Bit banged using the down counting PIT timers
4.	EBI	ADDR12	DDRA	PTA	PA4	YES	YES	NO	NO	NO	NO	External address bus		
3.	EBI	ADDR13	DDRA	PTA	PA5	YES	YES	NO	NO	NO	NO	External address bus		
1.	EBI	ADDR15	DDRA	PTA	PA7	YES	YES	NO	NO	NO	NO	External address bus	Fuel pump relay control	
47.	EBI	ROMCTL /EWAIT	DDRK	PTK	PK7	YES	YES	NO	NO	NO	NO	External address bus		
46.	EBI	ACC1/AD DR21	DDRK	PTK	PK5	YES	YES	NO	NO	NO	NO	External address bus	Second Stage injector out 6	Bit banged by piggy backing the main injector channels
45.	EBI	ACC0/AD DR20	DDRK	PTK	PK4	YES	YES	NO	NO	NO	NO	External address bus	Second Stage injector out 5	Bit banged by piggy backing the main injector channels
44.	EBI	IQSTAT3 /ADDR19	DDRK	PTK	PK3	YES	YES	NO	NO	NO	NO	External address bus	Second Stage injector out 4	Bit banged by piggy backing the main injector channels
43.	EBI	IQSTAT2 /ADDR18	DDRK	PTK	PK2	YES	YES	NO	NO	NO	NO	External address bus	Second Stage injector out 3	Bit banged by piggy backing the main injector channels
42.	EBI	IQSTAT1 /ADDR17	DDRK	PTK	PK1	YES	YES	NO	NO	NO	NO	External address bus	Second Stage injector out 2	Bit banged by piggy backing the main injector channels
41.	EBI	IQSTAT0 /ADDR16	DDRK	PTK	PK0	YES	YES	NO	NO	NO	NO	External address bus	Second Stage injector out 1	Bit banged by piggy backing the main injector channels
43 H1, 48 H2	XEBI ctrl	ECLKX2/ XCLKS	DDRE	PTE	PE7	YES	YES	NO	NO	NO	NO	System configuration	Uni-directional hardware flow control – SCI0	Using as input will result in random behaviour
JB1 : 4	XEBI ctrl	MODB/T AGHI	DDRE	PTE	PE6	YES	YES	NO	NO	NO	NO	System configuration		Using as input will result in random behaviour, output goes low during reset
JB1 : 3	XEBI ctrl	MODA/T AGLO/R E	DDRE	PTE	PE5	YES	YES	NO	NO	NO	NO	System configuration		Using as input will result in random behaviour, output goes low during reset
33 H1, 18 H2	XEBI ctrl	ECLK	DDRE	PTE	PE4	YES	YES	NO	NO	NO	NO	System configuration		
19.	XEBI ctrl	LSTRB/L DS/ERO MCTL	DDRE	PTE	PE3	YES	YES	NO	NO	NO	NO	System configuration		
17.	XEBI ctrl	R/W/WE	DDRE	PTE	PE2	YES	YES	NO	NO	NO	NO	System configuration		
46 H1, 20 H2	XEBI ctrl	IRQ	DDRE	PTE	PE1	NO	YES	NO	NO	NO	YES	IRQ	(with interrupt cabability)	
45.	XEBI ctrl	XIRQ	DDRE	PTE	PE0	NO	YES	NO	NO	NO	YES	XIRQ	(with interrupt cabability)	

Note
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Currently to adhere to GCC compatibility it is intended NOT to use the XGATE at all. However it would certainly be prudent to ensure that the pin choices are compatible with using XGATE in the future.

Future XGATE tasks : (100% open to suggestion)

- Serial SCI and/or SPI comms
- Software PWM